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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,517	09/27/2000	Richard K. Greicar	19223-001010US	2127

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EXAMINER
BAKER, PAUL A

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 03/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/672,517	Applicant(s) GREICAR, RICHARD K.	
	Examiner Paul A Baker	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-19 are presented for examination.

Priority

Receipt is acknowledged of papers submitted on 27 September 2000, under 35 U.S.C. § 119(e), which papers have been placed of record in the file.

Information Disclosure Statement

Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method and apparatus for a processor containing paged local and external memory.

The specification has omitted the application numbers for related co-pending applications. Page 16 line 12 should be amended with the serial number 09/678,858, also the title should be amended to "Method of Processing Data Utilizing Queue Entry." Page 16 line 13 should be amended with the serial number 09/678,898.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-6,8-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Hudson et al. US Patent 6,205,522.

In regards to claim 1, Hudson discloses a processor having a local memory for storing code in Figure 7 elements 432 and 418. Hudson discloses configuring the local memory into a plurality of blocks in Figure 17 element 318, subdivisions 1701-1703. Hudson discloses an external memory for use by the processor in Figure 7 element 404. Hudson discloses storing a program of code in external memory where the program code is segmented into blocks that can be stored in blocks of local memory in and in which a first block of code is stored in at least one block of memory in Figure 17.

In regards to claim 2, Hudson discloses storing a first block of code in local memory comprising of a plurality of blocks of memory in column 18 lines 9-12.

In regards to claim 3, Hudson discloses storing a second block of code in local memory in Figure 17 and in column 18 lines 9-19.

In regards to claim 4, Hudson discloses the DSP controlling the downloading of code into a local memory block in column 19 lines 5 through 8. Since the DSP controls the downloading of the code, it knows when the downloading has completed. The DSP transfers control to the downloaded code as described in column 18 lines 3 through 31.

In regards to claim 5, Hudson discloses determining that a block of code has completed and replacing the executed code block with another block of code in column 18 lines 25 through 28.

In regards to claim 6, Hudson disclose the storing of a first block of code from a second program in an available block of memory while the first program code is still executing in column 18 lines 20 through 24.

In regards to claim 8, Hudson discloses a processor, a local memory of the processor, and an external memory for use by processor in Figure 7 elements 432, 418, and 404. A program of code for processing by processor and where program of code is segmented into blocks of code that can be stored in corresponding memory blocks in Figure 17. Where memory requirements for storing the program of code are larger than a total potion of the local memory designated for storing the blocks of code in column 2 lines 39 through 42.

In regards to claim 9, Hudson discloses the use of a second local memory in column 16 lines 25 through 28.

In regards to claim 10, Hudson discloses the use of second local memory to store data for use by first local memory in column 16 lines 25 through 28.

In regards to claim 11, Hudson discloses the program of code being disposed in external memory in figure 17.

In regards to claim 12, Hudson discloses a second program of code for processing by the processor in Figure 17.

In regards to claim 13, Hudson discloses the storing of program code in a queue (buffer) for loading into the local memory in column 17 lines 32 through 36.

In regards to claim 14, Hudson discloses the storing of data within the queue (buffer) for loading into local data memory in column 20, lines 5 through 8.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hudson in view of Forin et al, US Patent 6,175,900.

In regards to claims 7 and 15, Hudson describes the applicant's invention substantially as claimed. However, Hudson does not disclose the use of a semaphore comprising of at least one bit for indicating when one block of the first local memory is available. Forin discloses the use of a bitmap, where each block of memory is represented by one or more bits to indicate, among additional information, whether a block of memory is available for use in the field of memory management of physical memory. The memory system disclosed by Hudson requires some method of keeping track of the current status of each block of local memory, while no method of management was specifically mentioned, the use of semaphores (or a bitmap with a depth of N bits as described by Forin, which is functionally equivalent to the use of a string of semaphores each of bit length N) was well known in the art, official notice is

taken. Therefore it would have been obvious at the time of invention to use a semaphore.consisting of one or more bits for the purpose of indicating the availability of one or more memory blocks.

In regards to claim 16, Hudson and Forin describe the applicant's invention substantially as claimed. Hudson further describes the inclusion of a second and third processor in Figure 6, elements 302 and 322' and stipulates the inclusion of additional units in column 4 lines 26 through 31. Hudson further states that his invention may specifically be used in multimedia systems such as DVD in column 1 lines 12 through 15 and column 4 lines 21 through 32. While Hudson does not explicitly divide the tasks among the processors it would be obvious to conclude that since Hudson explicitly describes a multiprocessor system capable of being used in a DVD system that he intended each processor to share the computational load. It also would have been obvious to separate the audio and video streams to be processed by two separate processors since these are easily separable data streams. It further would have been obvious to assign the third processor to the task of communicating with the DVD media device and receive the raw DVD data stream for the eventual processing by the other two processors. Therefore it would have been obvious at the time of invention to include a second processor for receiving a stream of data formatted for use by a DVD player, a third processor for processing video components of the stream DVD data and the first processor processing the audio component of the stream of the DVD data.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett, US Patent 5,579,520, in view of Hudson, US Patent 6,205,522.

In regards to claim 17, Bennett discloses a method of preparing program code for use by a processor having limited local memory in Figure 1c and Figure 5. Bennett discloses determining the fundamental memory block size of local memory and segmenting the program of code into a plurality of blocks of code in claim 25. Bennett, however, does not disclose the storing of said block of code into and external memory separate for the processor. Hudson discloses the storing of said blocks in an external memory separate from said processor in column 4 lines 36-41. Hudson discloses the use of a paged memory system with a processor having limited local memory, while Bennett discloses the preparation of computer code for use of a paged memory system on a processor system having limited local memory. These two inventions represent the two sides of the same coin, i.e. each requires the existence of the other. Therefore it would have been obvious at the time of invention to combine the preparation of code for limited local memory processor system with the functionality of the system itself.

In regards to claim 18, Bennett and Hudson disclose the invention substantially as claimed. Hudson further discloses the system further comprising the placement of blocks of code for loading into a queue (buffer) for loading into the local memory of the processor in column 17 lines 32 through 36.

In regards to claim 19, Bennett and Hudson disclose the invention substantially as claimed. Hudson further discloses the use of a second program in column 18 lines 15 through 19, since this program also must undergo the process of segmentation and the second program would also be placed on the queue (buffer) for placement into local memory as described in column 17 lines 32 through 36. It would have been obvious at

the time of invention to one skilled in the art to prepare a second program of code by segmenting the code and arranging the blocks of code into the queue (buffer).

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1-19 provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-19 of copending Application No. 09/678858. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Douceur et al. US Patent 5,903,917 teaches the division of code into memory page blocks taking into consideration alignment requirements.

Little US Patent 4,947,477 teaches a processing system where both data and program memory are partitionable.

Yagi US Patent 6,240,497 teaches the allocation of memory between program and data segments.

Kohn US Patent 5,276,847 teaches a method of locking and unlocking a computer address.

Inagami et al. US Patent 5,109,499 teaches the access of multi-vector processors with a common vector register.

Frank et al. US Patent 5,335,325 teaches multiple processors connected to a common content addressable memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on (703)308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7238 for regular communications and (703)746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

PB
February 28, 2002

DOHYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application